IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

COMPUTER CIRCUIT OPERATIONS LLC, Plaintiff -against- SOCIONEXT INC. Defendant	**Case No.: 6:20-cv-00046** **Jury Trial Demanded**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Computer Circuit Operations LLC ("CCO"), for its Complaint against Defendant Socionext Inc. (collectively "Socionext" or "Defendant"), hereby alleges as follows:

PARTIES

1. Plaintiff CCO is a limited liability company organized and existing under the laws of the State of New York, having its principal place of business at 1629 Sheepshead Bay Road, Floor 2, Brooklyn, New York, 11235.

2. Socionext Inc. is a corporation organized under the laws of Japan with its principal place of business at Nomura Shin-Yokohama Bldg., 2-10-23 Shin-Yokohama, Kohoku-ku, Yokohama, Kanagawa, 222-0033, Japan.

JURISDICTION AND VENUE

3. This is an action under the patent laws of the United States, 35 U.S.C. §§ 1, et seq., for infringement by Socionext of claims of U.S. Patent Nos. 6,480,021, 6,820,234, 7,107,386, 7,278,069, and 7,426,603 ("the Patents-in-Suit").

4. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

5. Socionext is subject to personal jurisdiction of this Court because, inter alia, on

information and belief, independently and/or via its agents, (i) Socionext sells and offers for sale its products in Texas, (ii) Socionext sells and offers for sale its products by using distributors and sales representatives located in Texas; and/or (iii) Socionext places its products in the stream of commerce with intent or knowledge that those products would end up in Texas. For example, Socionext sells its systems on chip (SoCs) to GoPro and other camera manufacturers with knowledge and intent that the products incorporating those SoCs would be sold in Texas and/or residents of Texas.

6. Venue is proper in this district under 28 U.S.C. § 1391(c) because, *inter alia*, Socionext is a foreign entity.

BACKGROUND

7. On November 12, 2002, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,480,021 ("the '021 Patent"), entitled "Transmitter Circuit Comprising Timing Deskewing Means."

8. Alexander Roger Deas, Vasily Grigorievich Atyunin, and Igor Anatolievich Abrossimov, invented the technology claimed in the '021 Patent.

9. On November 16, 2004, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,820,234 ("the '234 Patent"), entitled "Skew Calibration Means And A Method Of Skew Calibration."

10. Alexander Roger Deas, Ilya Valerievich Klotchkov, Igor Anatolievich Abrossimov, and Vasily Grigorievich Atyunin invented the technology claimed in the '234 Patent.

11. On September 12, 2006, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,107,386 ("the '386 Patent"), entitled "Memory Bus Arbitration Using Memory Bank Readiness."

12. Stephen Clark Purcell and Scott Kimura invented the technology claimed in the '386

Patent.

13. On October 2, 2007, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,278,069 ("the '069 Patent"), entitled "Data Transmission Apparatus For High-Speed Transmission Of Digital Data and Method For Automatic Skew Calibration."

14. Igor Anatolievich Abrosimov, Vasily Grigorievich Atyunin, Alexander Roger Deas, and Ilya Vasilievich Klotchkov invented the technology claimed in the '069 Patent.

15. On September 16, 2008, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,426,603 ("the '603 Patent"), entitled "Memory Bus Arbitration Using Memory Bank Readiness."

16. Stephen Clark Purcell and Scott Kimura invented the technology of the '603 Patent.

17. CCO is the assignee and owner of the right, title, and interest in and to the Patents-in-Suit, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement.

NOTICE

18. By letter dated May 23, 2019, CCO notified Socionext of the existence of the Patents-in-Suit, and of infringement of the '234, '386, '069, and '603 Patents by Socionext. CCO's letter identified exemplary infringing Socionext products and an exemplary infringed claim for each of the '234, '386, '069, and '603 Patents. CCO's May 23, 2019 letter invited Socionext to hold a licensing discussion with CCO. Socionext received the May 23, 2019 letter on May 29, 2019.

19. CCO notified Socionext of the '021 Patent in the May 23, 2019 letter and, at least as of the time of the filing of this complaint, Socionext has had notice of its infringement of the '021 Patent.

LICENSING

20. As of the time of this complaint, CCO has entered into licensing agreements relating to

the Patents-in-Suit with at least Arastu Systems, NVIDIA, and Qualcomm.

COUNT I: INFRINGEMENT OF THE '021 PATENT

21. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

22. On information and belief, Socionext has infringed the '021 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States processors, microcontrollers, and gateways identified in Attachment 1 ("Accused Socionext Products") that include DDR3, DDR4, LPDDR3, LPDDR4, and/or LPDDR4x controller ("DDR Controller").

23. On information and belief, Socionext has infringed at least claim 11 of the '021 Patent by performing a method of eliminating skew caused by inter-symbol interference and cross-talk influence in the transmission line for high-speed transmission of digital data by modifying delays at each DQ line of an exemplary DDR Controller, such as an LPDDR4 Controller incorporated in the Accused Socionext Products, including during regular operation and during development, design, testing, and verification of the Accused Socionext Products. *See* Ex. 1, Socionext, Custom SOC (ASIC), Nov. 2019, p. 27; Ex. 2, JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017, p. 195. The DDR Controller continuously transmits data through each DQ transmission line during centering and link training. *See* Ex. 1 at 27 ("DFI compliant (all macro)"; "the PHY function (training function)."); *See* Ex. 2 at 195 ("Up to 5 consecutive MPC [Write DQ FIFO] command with user defined patterns may be issued to the SDRAM to store up to 80 values (BL16 x5) per pin that can be read back via the MPC [Read DQ FIFO] command.") The DDR Controller measures a skew for the transmitted DQ bit patterns by training write boundaries of a data eye during write leveling. *See id.* ("After writing data to the SDRAM with the MPC [Write DQ FIFO] command, the data can be read back with the MPC][Read DQ FIFO] command and results compared with "expect" data to see if further training (DQ delay) is needed."). The DDR

Controller records and stores information on skew caused by inter-symbol interference and cross-talk influence in the DQ transmission lines for at least one data pattern transmitted through the transmission line. *See id.* The DDR Controller generates and applies a correction to the timing position of a signal transition between two logical levels, the correction being generated on the basis of the information stored in the storage means, so as to compensate for the above skew. *See id.*; *see also id*. at 200.

24. On information and belief, Socionext has induced, and continues to induce, infringement of the '021 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Socionext Products that incorporate the DDR Controller. Socionext had the knowledge of the '021 Patent, at least from the time of filing this complaint, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Socionext Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

25. On information and belief, Socionext has committed the foregoing infringing activities without a license.

26. On information and belief, Socionext's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

COUNT II: INFRINGEMENT OF THE '234 PATENT

27. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

28. On information and belief, Socionext has infringed the '234 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling

in the United States, or importing into the United States the Accused Socionext Products.

29. For example, on information and belief, Socionext has infringed at least claim 28 of the '234 Patent by making, using, offering to sell, selling in the United States, or importing into the United States the Accused Socionext Products that include the DDR Controller with a timing uncertainty reduction system for calibration of a high speed communication apparatus, including during development, design, testing, and verification of the Accused Socionext Products and specifically the DDR Controller. Ex. 1 at 27. An exemplary DDR Controller reduces timing uncertainty in LPDDR4/x memory transmission including calibration using the Multi-Purpose Register (MPR), read centering, write centering, and write leveling. *See* Ex. 2, JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017, pp. 26, 190, 195. *See also* Ex. 3, DDR PHY Interface, DFI 4.0 Specification, p. 55. The DDR Controller comprises at least one driving register for latching transmitted DQ signals, with a plurality of input and outputs. The DDR Controller further comprises at least one receiving register for latching received DQ signals, with a plurality of inputs and outputs. The DDR Controller DMCs include a main clock for generating a main clock signal (such as the MC Clock). *See id*. at 120 ("The MC clock is always the DFI clock and all DFI signals are referenced from the MC clock."). The DDR Controller includes a reference clock, such as an internal clock or a PHY clock, for generating a reference signal for calibrating the receiving register or registers, such as during DQ read centering/read training. The reference clock is associated with the main clock signal. *See id.* at 16, 120; Ex. 2, JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017, pp. 190, 195. The DDR Controller includes phase shift circuitry to align the timing of the driving signals' relative to the CK signal at the destination. For example, the phase shift circuitry aligns the timing of the DQS signals via write leveling. *See id*. at 186 ("To improve signal-integrity performance, the LPDDR4 SDRAM provides a

write-leveling feature to compensate CK-to-DQS timing skew affecting timing parameters such as tDQSS, tDSS, and tDSH. The DRAM samples the clock state with the rising edge of DQS signals, and asynchronously feeds back to the memory controller. The memory controller references this feedback to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair"); Ex. 3, DDR PHY Interface, DFI 4.0 Specification, p. 157.

30. On information and belief, Socionext has induced, and continues to induce, infringement of the '234 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Socionext Products that incorporate the DDR Controller. Socionext had the knowledge of the '234 Patent and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Socionext Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

31. On information and belief, Socionext has committed the foregoing infringing activities without a license.

32. On information and belief, Socionext's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

33. On information and belief, Socionext knew the '234 Patent existed, knew of an exemplary infringed claim of the '234 Patent, and knew of exemplary infringing Socionext products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '234 Patent.

COUNT III: INFRINGEMENT OF THE '386 PATENT

34. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

35. On information and belief, Socionext has infringed the '386 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the Accused Socionext Products.

36. For example, on information and belief, Socionext has infringed at least claim 1 of the '386 Patent by making, using, offering to sell, selling in the United States or importing into the United States the Accused Socionext Products, which include a DDR Controller, adapted to send a plurality of memory transactions over a memory bus to a memory having a plurality of memory banks. *See, e.g.*, Ex. 1 at 27, 30. Exemplary DDR Memory to which the DDR Controller connects has multiple memory banks. *See id*. at 18. *See* e.g., Ex. 4, JEDEC STANDARD DDR3 SDRAM JESD79-3C (Revision of Jesd79-3B, April 2008) at p. 15-16. The Socionext Products send the requests over a memory bus. Ex. 1 at 27 ("Bus switching verification: Optimizes the write and read bus switch timing"). The DDR Controller comprises a queue comprising a plurality of request stations for storing memory transactions, such as read requests, such as a command queue FIFO. *See id* at 27. Each of the memory transactions is addressed to one of the memory banks. *Id.* at 18. *See also* Ex. 4 at 33. The DDR Controller includes an arbiter, such as the memory controller IP block. *See* Ex. 1 at 27 ("Memory controller IP • Controller for maximizing high DRAM utilization"). The arbiter is simultaneously coupled to each of the request stations and adapted to select any of the memory transactions. *See id.* The arbiter is configured to generate a plurality of bank readiness signals, such as following the submission of an activate command to the DDR3 memory. *See also* Ex. 4 at 18, 55. The DDR Controller, based on the bank readiness signals, is configured to select one of the memory transactions for transmission over the memory bus. *See* Ex. 1 at 18.

37. On information and belief, Socionext has induced, and continues to induce, infringement of the ’386 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Socionext Products. Socionext had the knowledge of the ’386 Patent and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Socionext Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

38. On information and belief, Socionext has committed the foregoing infringing activities without a license.

39. On information and belief, Socionext’s infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

40. Socionext knew the ’386 Patent existed, knew of its claims, and knew of Socionext infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the ’386 Patent.

COUNT IV: INFRINGEMENT OF THE ’069 PATENT

41. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

42. On information and belief, Socionext has infringed the ’069 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States the Accused Socionext Products.

43. For example, on information and belief, Socionext has infringed at least claim 12 of the ’069 Patent by performing a method for automatic skew calibration of a transmission apparatus for high speed transmission of digital data, including during development, design, testing, and

verification of the Accused Socionext Products, which include the DDR Controller, such as a LPDDR4/4x memory controller that automatically calibrates skew of LPDDR4/4x DDRs. *See* Ex. 1 at 27; Ex. 2 at 26. The DDR Controller initiates Write Leveling and Read Optimization via the PHY. *See id*. The PHY comprises a transmitter and the receiver. Socionext calibrates registers of the receiver, such as the PHY registers in relation to a reference clock edge, such as a PHY clock. *See* Ex. 3, DDR PHY Interface, DFI 4.0 Specification, pp. 16, 17, 25, 147. Socionext calibrates propagation delays of registers of the transmitter, using the calibrated registers of the receiver with the Write Leveling feature. *See* Ex. 2 at 186 ("To improve signal-integrity performance, the LPDDR4 SDRAM provides a write-leveling feature to compensate CK-to-DQS timing skew affecting timing parameters such as tDQSS, tDSS, and tDSH. The DRAM samples the clock state with the rising edge of DQS signals, and asynchronously feeds back to the memory controller. The memory controller references this feedback to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair"); Ex. 3 at 157. The calibration is performed by measuring time offsets between different signals that form a communication channel, including the DQS_t-DQS-c and CK_t-CK_c signals. The calibration is performed for a plurality of data patterns, such as DQS_t – DQS_c patterns with variable delays. Ex. 2 at 186. ("5. The feedback provided by the DRAM is referenced by the controller to increment or decrement the DQS_t and/or DQS_c delay settings. 6. Repeat step 4 through step 5 until the proper DQS_t/DQS_c delay is established."). Socionext applies the measured time offsets to compensate for the inter-signal skew by performing relative alignment of the measured offsets to a main clock edge. *See id.*; Ex. 3 at 144-145.

44. On information and belief, Socionext has induced, and continues to induce, infringement of the '069 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing,

causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Socionext Products that incorporate the DDR Controller. Socionext had the knowledge of the '069 Patent and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Socionext Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

45. On information and belief, Socionext has committed the foregoing infringing activities without a license.

46. On information and belief, Socionext's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

47. On information and belief, Socionext knew the '069 Patent existed, knew of an exemplary infringed claim of the '069 Patent, and knew of exemplary infringing Socionext products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '069 Patent.

COUNT V: INFRINGEMENT OF THE '603 PATENT

48. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

49. On information and belief, Socionext has infringed the '603 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the Accused Socionext Products.

50. For example, on information and belief, Socionext has infringed at least claim 14 of the '603 Patent by performing a method of using a multiplexer to manage the transmission of a plurality of memory transactions to a memory having a plurality of memory banks, including

during development, design, testing, and verification of the Accused Socionext Products. The DDR Controller of the Accused Socionext Products use a multiplexer. *See* Ex. 1 at 27 (Inter Connect connecting to various blocks such as CPU Block, Storage Block, etc. as inputs). Memory to which the Accused Socionext Products connect has multiple memory banks. See e.g., Ex. 4, JEDEC STANDARD DDR3 SDRAM JESD79-3C (Revision of Jesd79-3B, April 2008) at p. 15-16. The multiplexer used by the DDR Controller comprises a plurality of multiplexer inputs for receiving the plurality of memory transactions, such as the inputs from CPU Block, Storage Block, Network Block, etc. *See* Ex. 1 at 27. The multiplexer also comprises a multiplexer output for sending each of the plurality of memory transactions to the memory, such as the interface to the DDR PHY. Socionext receives a plurality of memory transactions at the multiplexer inputs. Each of the memory transactions is addressed to a corresponding memory bank. *See* Ex. 4 at p. 33. The DDR Controller associates a priority with each received memory transaction. Ex. 1 at 27. ("High performance QoS-Arbiter featuring multiple functions"). The DDR Controller generates a plurality of bank readiness signals indicating the readiness of each memory bank available to accept a memory transaction, such as following the submission of activate commands to the DDR3 memory. *See* Ex. 4 at 18, 55. The bank readiness signals are based on the plurality of memory transactions at the multiplexer inputs and the multiplexer output. The DDR Controller sends each of the plurality of memory transactions to its corresponding memory bank via the DRAM PHY based on the associated priorities and the bank readiness signals. *See* Ex. 1 at 27 ("Bus switching verification : Optimizes the write and read bus switch timing."); *see also id.* at 18 (showing "Efficient Memory Access.").

51. On information and belief, Socionext has induced, and continues to induce, infringement

of the ’603 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, Accused Socionext Products. Socionext had the knowledge of the ’603 Patent and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Socionext Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

52. On information and belief, Socionext has committed the foregoing infringing activities without a license.

53. On information and belief, Socionext’s infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

54. Socionext knew the ’603 Patent existed, knew of its claims, and knew of Socionext’s infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the ’603 Patent.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff CCO prays for the judgment in its favor against Socionext, and specifically, for the following relief:

A. Entry of judgment in favor of CCO against Socionext on all counts;

B. Entry of judgment that Socionext has infringed the Patents-in-Suit;

C. Entry of judgment that Socionext’s infringement of the ’234, ’386, ’069, and ’603 Patents has been willful;

D. Award of compensatory damages adequate to compensate CCO for Socionext’s infringement of the Patent-in-Suit, in no event less than a reasonable royalty trebled as provided

by 35 U.S.C. § 284;

E. Award of CCO's costs;

F. Pre-judgment and post-judgment interest on CCO's award; and

G. All such other and further relief as the Court deems just or equitable.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Fed. R. Civ. P., Plaintiff CCO hereby demands trial by jury in this action of all claims so triable.

Dated: January 22, 2020

Respectfully submitted,

/s/ Dmitry Kheyfits

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ATTACHMENT 1

M9M
MB86M31
MB86M30
SC2M50
M820L
SC1400A
SC1401A
SC1408A
SC1405AP1 (LD11)
MN2WS0270 (sLD8)
SynQuacer S-Series SC2A11
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SC2000 M10V
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